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EAST Browser - L2: (47) 1 not active :: | US 5886353 | Tag: S,T1 | Doc: 14/47 (SORTED) | "Full" 16/43 (Total images 43)

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32, column-select shift register 36, sixteen
sixteen bilateral switches 56.

(11) The voltage on capacitor 24 of each
recorded by the readout circuit 18 in the fol
row (1.1, 1.2, . . . , 1.16) of pixel circuits 11
shift register 32 activates row-select line 53
selection transistor 30 of each pixel 11 in th
comprised of two conventional inverter circ
the first row is then sequentially and non-de
First, the voltages on column readout line 2
(1.1, 1.2, . . . , 1.16) are simultaneously sa
sample-and-hold circuit 54, when a digital s
sample-and-hold circuits 54 at line 37. Thi
voltage at the output line 55 of each sampl
below) which is identical to the voltage at e
for a small (approximately 1 Volt) positive v
voltages at output lines 55 sampled by the
are sequentially connected to the output lin
controlled by column-select shift register 36

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		20030021373 06 A1		
14		US 5886353 A	199903 23	Imaging
15	☑	US 2002012543	200209 12	Imaging

Details | Text | Image | HTML

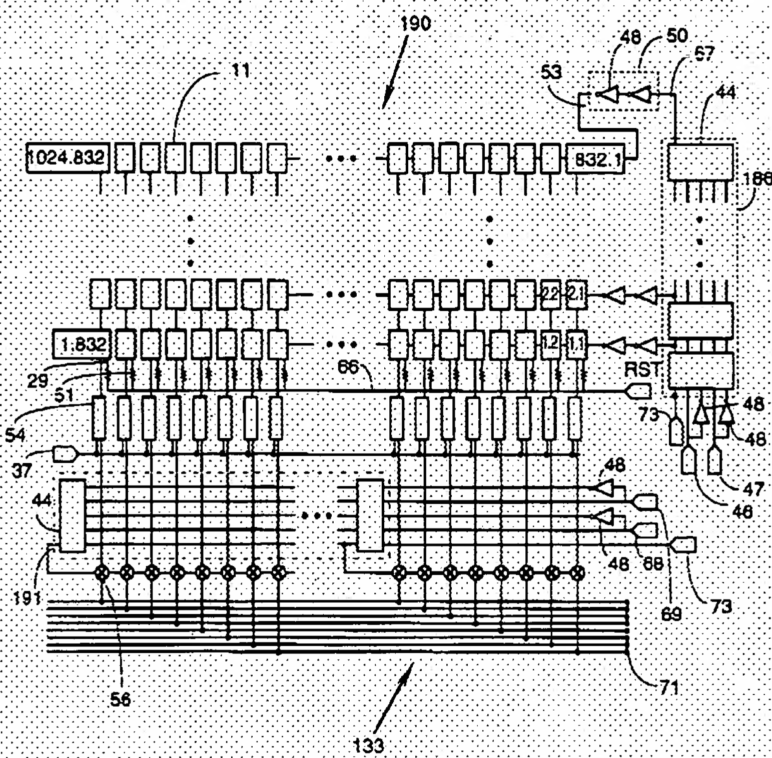

FIG. 16

Details | Text | Image | HTML | Full

EAST Browser - L3: (70) 2 AND ((348/... | US 20020181648 | Tag: S.T1 | Doc: 27/70 (SORTED) | "Full" 5/15 (Total images 15)

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DOCUMENT-IDENTIFIER: US 2002018

TITLE: Exposure control in an x-

---------- KWIC ---------

Current US Classification, US Primary Clas
378/19

Summary of Invention Paragraph - BSTX (
[0016] The pixels may be arranged in row
sharing a row address line and columns of
wherein the charge storage element is con
device between a common electrode for all
the switching device being controlled by the

Details | Text | Image | HTML | KWIC

	U	Document I	Issue D	
25	☐	US 5068701 A	199111 26	Device fo supplied substrate
26	☐	US 4679085 A	198707 07	Digital in and audi
27	☐	US 2002018164 8 A1	200212 05	Exposure
28	☑	US 5648654 A	199707 15	Flat pane electrode

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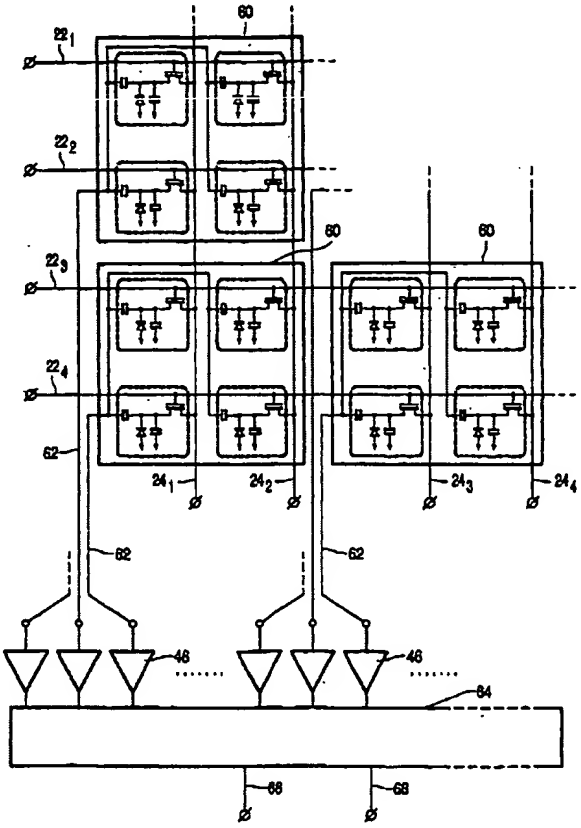

FIG. 5

Details | Text | Image | HTML | Full

EAST Browser - L3: (70) 2 AND ((348/.. | US 6243441 | Teq: S,T1 | Doc: 3/70 (SORTED) | "Full" 4/32 (Total images 32)

File Edit View Tools Window Help

US-PAT-NO: 6243441

DOCUMENT-IDENTIFIER: US 6243441 B

TITLE: Active matrix detector for

---------- KWIC ---------

Brief Summary Text - BSTX (25):

Further in accordance with a preferred er real-time radiation data is read out at a first from the cluster data output lines, and integ at a second spatial resolution from the com sequential row-by-row matrix addressing of Additionally, the real-time radiation data is control.

Details | Text | Image | HTML | KWIC

	U	Document I	Issue D	
1	☐	US RE34908 E	199504 18	3-transis 2-dimens
2	☐	US 5083016 A	199201 21	3-transis 2-dimens
3	☐	US 6243441 B1	200106 05	Active m
4	☑	US 5949483 A	199909 07	Active pi

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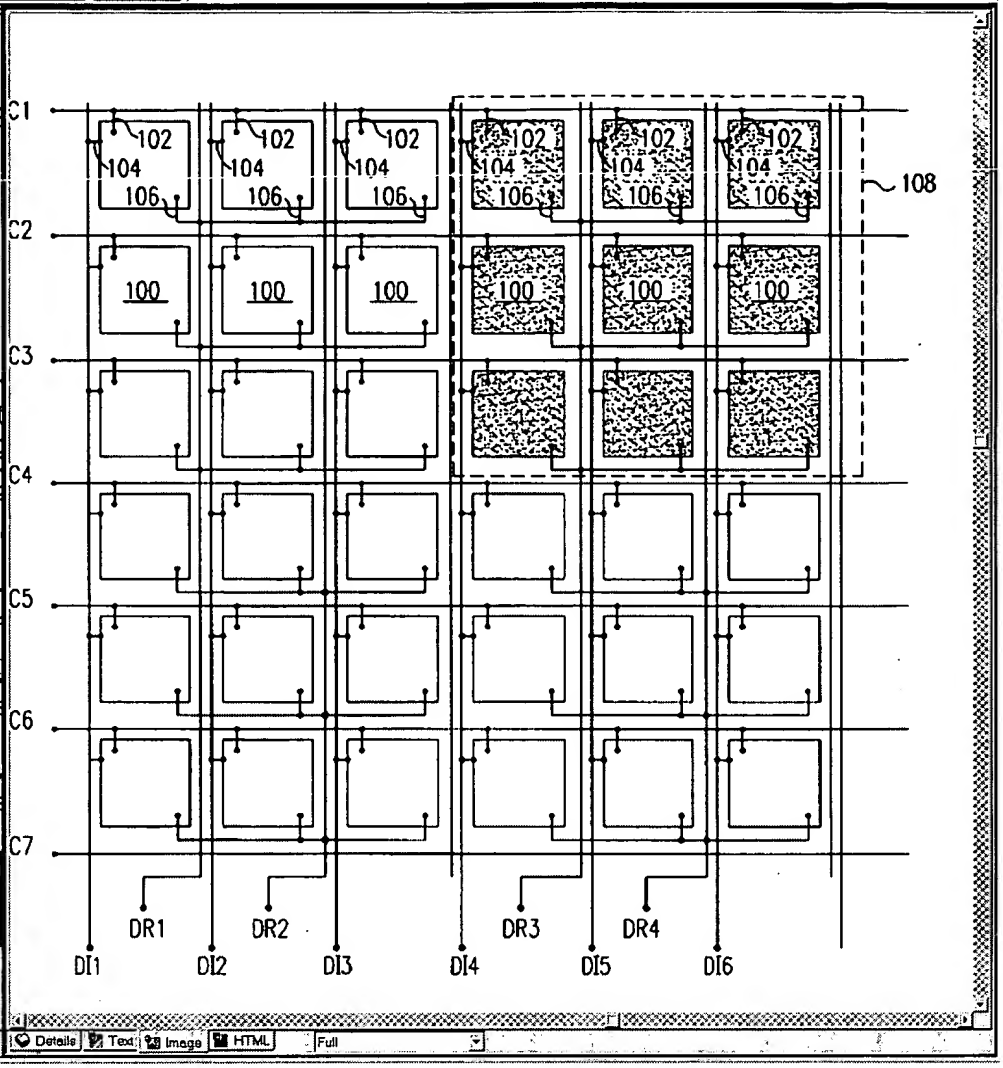


Details | Text | Image | HTML | Full

US-PAT-NO: 6535576

DOCUMENT-IDENTIFIER: US 6535576 B

TITLE: Enhanced digital detector incorporating same

DATE-ISSUED: March 18, 2003

INVENTOR-INFORMATION:

NAME	CITY
Vafi; Habib	Brookfield
Petrick; Scott W.	Sussex
Perry; Douglas I.	Ottawa

ASSIGNEE INFORMATION:

NAME	CITY	STA CODE
GE Medical Systems	Waukesha	

	U	Document I	Issue D	
1	☐	US 20020085670 A	200303 18	Digital de couples read-out
2	☐	US 6535576 B2	200303 18	Enhance incorpora

FIG. 5

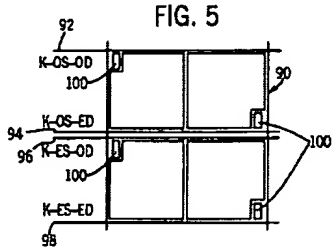
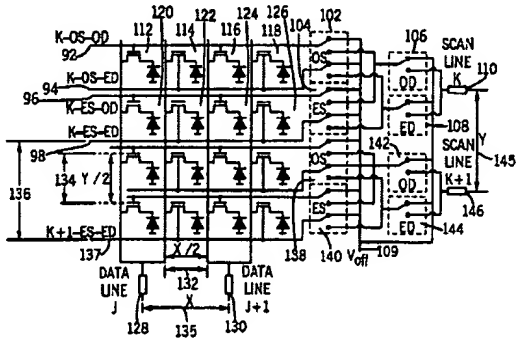
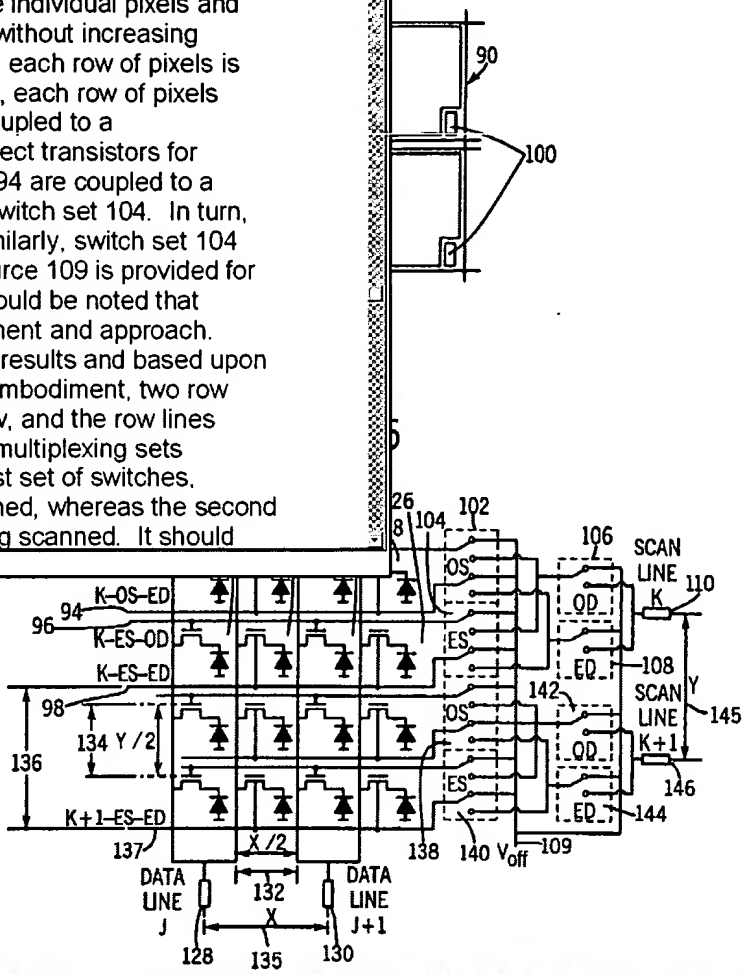


FIG. 6



(16) FIG. 6 represents, in somewhat greater detail, the individual pixels and the multiplexing circuitry utilized to increase pixel pitch without increasing the interconnect density. In the illustrated embodiment, each row of pixels is connected to a row line 92, 94, 96, and 98. Specifically, each row of pixels is coupled to two row lines. Further, each row line is coupled to a multiplexer having solid state switches, such as field effect transistors for selective row enabling. For instance, row lines 92 and 94 are coupled to a switch set 102, and row line 96 and 98 are coupled to switch set 104. In turn, switch set 102 is coupled to switches 106 and 108. Similarly, switch set 104 is also coupled to switches 106 and 108. A voltage source 109 is provided for disabling the pixels in the matrix via the switches. It should be noted that this embodiment illustrates only one scanning arrangement and approach. However, different approaches may be used for similar results and based upon the present technique. For example, in this particular embodiment, two row lines are coupled to alternate pixels within the same row, and the row lines are coupled to two individual switches within the same multiplexing sets operated to scan that particular row. In addition, the first set of switches, when enabled, selects the column of pixels being scanned, whereas the second set of switches enables the particular row of pixels being scanned. It should



	U	Document I	Issue D	
1	☐	US 2002008567 0 A	200303 18	Digital de couples read-out
2	☐	US 6535576 B2	200303 18	Enhance incorpora

DOCUMENT-IDENTIFIER: US 20020171102 A1

TITLE: Non-volatile solid state image pickup device and its drive

--------- KWIC ---------

Detail Description Paragraph - DETX (11):

[0053] As shown in FIG. 1(A), a sample hold circuit S/H, AD converter A/D, etc., for digitizing the threshold voltage are also provided on-chip on semiconductor substrate 10. The data that have been subject to AD conversion are recorded in latch circuit LT, read out successively in the horizontal direction by horizontal shift register SR, and output via output buffer amplifier AMP to the exterior of the image pickup device as digital data.

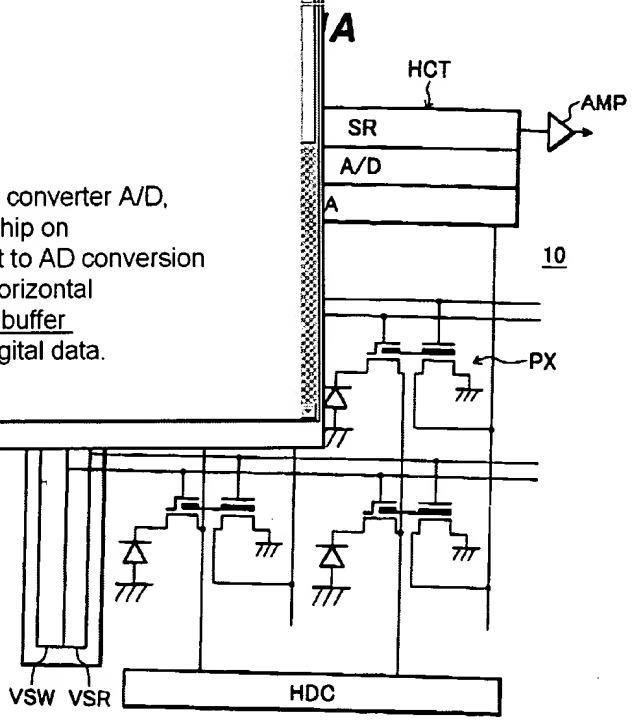


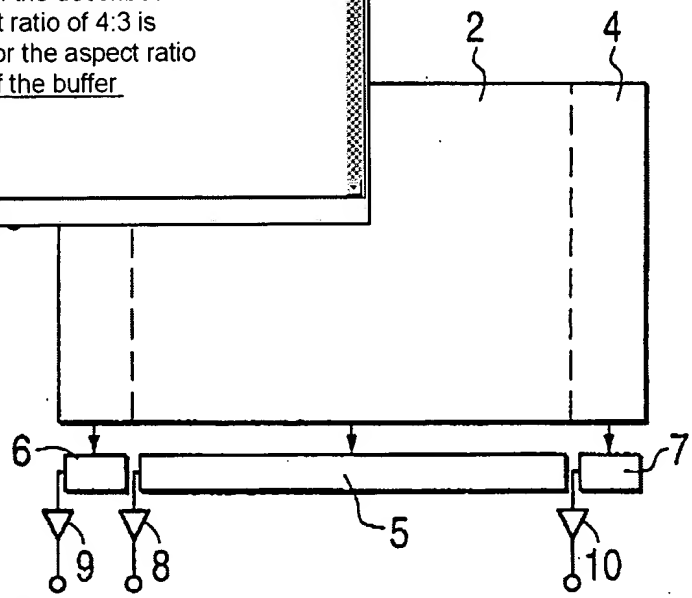
FIG.1B

	U	Document I	Issue D	
1		US 5091784 A	199202 25	Matrix ty non-inter
2		US 2002017110 2 A1	200211 21	Non-vola drive
3		US 5491512 A	199602 13	Solid sta method
4		US 5483283 A	199601 09	Three le sensor

Brief Summary Text - BSTX (7):

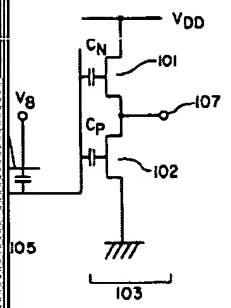
For both aspect ratios of 4:3 and 16:9, signal charges are read out from the imaging region 1 to the vertical shift registers in the first place. Then, vertical transfer signals are applied to the vertical shift registers from terminals A1-A4 to transfer the signal charges accumulated in the groups of photosensitive elements in said first segment 2, second segment 3 and third segment 4 to said first horizontal shift register 5, second horizontal shift register 6 and third horizontal shift register 7, respectively. Then, horizontal transfer pulses are applied to the respective horizontal shift registers to transfer the signal charges therein to the corresponding buffer amplifiers 8, 9 and 10 to thereby output picture signals. In the described arrangement, a picture signal corresponding to the aspect ratio of 4:3 is available from the buffer amplifier 8 and a picture signal for the aspect ratio of 16:9 is obtained by superimposing the signal outputs of the buffer amplifiers 8, 9 and 10 in an external circuit.

FIG. 1
PRIOR ART



	U	Document I	Issue D	
1	☐	US 5091784 A	199202 25	Matrix ty non-inter
2	☐	US 2002017110 2 A1	200211 21	Non-vola drive
3	☐	US 5491512 A	199602 13	Solid sta method
4	☑	US 5483283 A	199601 09	Three le sensor

FIG. 1 is a circuit diagram showing a first embodiment of the present invention. Reference 101 indicates a N channel MOS transistor, while reference 102 indicates a P channel MOS transistor; both of these are depression type transistors. Transistors 101 and 102 form a push pull type amplifier, that is to say, a CMOS type source follower circuit 103. Reference 104 indicates a gate electrode common to MOS transistors and 102; this may comprise, for example, a first layer multi-crystalline silicon layer. This serves as the input electrode for source follower circuit 103, and is connected to signal input terminal V.sub.9, via switching element 105. This switching element may employ a single NMOS or PMOS, for example, or may comprise a pair of NMOS and PMOS arranged in parallel, or a so-called CMOS switch. C.sub.N and C.sub.P, indicate capacities, between the channels and gate electrode 104, of NMOS 101 and PMOS 102, respectively. References 106a-106c and the like indicate input gate electrodes; these may comprise, for example, second layer multi-crystalline silicon layers. Furthermore, these input gates are connected to input signal terminals V.sub.1 -V.sub.8. If the floating potential of the common gate electrode 104 in the state in which switch 105 is open is represented by V.sub.F, then V.sub.F is given by the following formula.



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	U	Document I	Issue D	
1	☐	US 6120461 A	200009 19	Apparatu scanning
2	☐	US 2003000708 3 A1	200301 09	Charge r
3	☐	US 6606119 B1	200308 12	Semicon
4	☑	US 5818526 A	199810 06	Solid sta vertical s

Details | Text | Image | HTML

I_1	I_2	I_3	Picture Element
I_8	I_9	I_4	
I_7	I_6	I_5	

Fig. 2

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